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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,498	03/24/2004	David John Butcher	550-541	4617
23117	7590	06/07/2006	EXAMINER	
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			LI, AIMEE J	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/807,498	Applicant(s) BUTCHER ET AL.	
	Examiner Aimee J. Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2004 and 29 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-60 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-60 is/are rejected.
- 7) ☒ Claim(s) 1-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/24/04; 9/21/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-60 have been considered. Claims 5-8, 10, 12-15, 18, 20-23, 25, 27-30, 33, 35-38, 40, 42-45, 48, 50-53, 55, and 57-60 have been amended by Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Specification, Drawings, and Abstract as received on 24 March 2004; IDS as received on 24 March 2005; Preliminary Amendment as received 29 July 2004; Power of Attorney as received on 29 July 2004; Oath and Declaration as received on 29 July 2004; and IDS as received on 21 September 2005.

Drawings

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings are hard-drawn or contain handwritten elements/language. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

4. Claims 1-15 are objected to because of the following informalities: Please correct the preambles from "Apparatus..." to read --An [[A]]apparatus...--. Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 31 and 46 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 31 and 46 are for “A computer program product including a computer program...” and the body of the claims are geared towards the functionality of the instructions. There is no tangible machine or composition of matter in the claim. “A computer program product including a computer program...” includes a piece of paper, since there is no limiting factor within the specification or claim language to exclude non-tangible subject matter.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 6-11, 14-15, 16, 21-26, 29-30, 31, 36-41, 44-45, 46, 51-56, and 59-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Click, Jr. et al., U.S. Patent Number 6,363,522 (herein referred to as Click) in view of Smith et al., U.S. Patent Number 5,430,862 (herein referred to as Smith).

9. Referring to claims 1, 16, and 31, taking claim 1 as exemplary, Click has taught an apparatus for processing data comprising:

a. Wherein said instruction decoder is responsive to a memory access instruction:

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- i. To compare a base register value stored within a base register specified by a base register field of said memory access instruction with a predetermined null value (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7); and
- ii. If said base register value matches said predetermined value, then to branch to execution of a null value exception handler (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7).

10. Click has not explicitly taught

- a. Processing logic operable to perform data processing operations; and
- b. An instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions.

11. However, Click has taught that the memory access instructions are executed on a processor, as shown in Figure 5, but provides no details about the “N Processor”. Smith has taught

- a. Processing logic operable to perform data processing operations (Smith column 2, line 53 to column 4, line 43; Figure 1; and Figure 2); and
- b. An instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions (Smith column 2, line 53 to column 4, line 43; Figure 1; and Figure 2).

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12. A person of ordinary skill in the art at the time the invention was made, and as taught by Smith, would have recognized that the processor of Smith increases performance and compatibility by allowing instructions from multiple instruction sets execute (Smith column 1, lines 36-39) and reducing the need to access off-chip memory (Smith column 2, lines 13-24). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the processor of Smith in the device of Click to increase processor performance and compatibility.

13. Claims 16 and 31 have similar limitations to claim 1 and are rejected for similar reasons. The only differences are that claim 16 is for a method and claim 31 is for a computer program product.

14. Referring to claim 46, Click has taught a computer program product including a computer program having native program instructions, said native program instructions comprising:

- a. A memory access instruction decodable by said instruction decoder to control said processing logic:
 - i. To compared a base register value stored within a base register specified by a base register field of said memory access instruction with a predetermined null value (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7); and
 - ii. If said base register value matches said predetermined value, then to branch to execution of a null value exception handler (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7).

15. Click has not explicitly taught a computer program product including a computer program operable to translate non-native program instructions to form native program instructions directly decodable by an apparatus for processing data having processing logic operable to perform data processing operations and an instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions. However, Click has taught that the memory access instructions are executed on a processor, as shown in Figure 5, but provides no details about the "N Processor". Smith has taught a computer program product including a computer program operable to translate non-native program instructions to form native program instructions directly decodable by an apparatus for processing data having processing logic operable to perform data processing operations and an instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions. (Smith column 2, line 53 to column 4, line 43; Figure 1; and Figure 2). A person of ordinary skill in the art at the time the invention was made, and as taught by Smith, would have recognized that the processor of Smith increases performance and compatibility by allowing instructions from multiple instruction sets execute (Smith column 1, lines 36-39) and reducing the need to access off-chip memory (Smith column 2, lines 13-24). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the processor of Smith in the device of Click to increase processor performance and compatibility.

16. Referring to claims 6, 21, 36, and 51, taking claim 6 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, wherein said null value exception handler is

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operable to determine if said memory access instruction attempting to access a location corresponding to a null value corresponds to emulation of a non-native program instruction that is not directly decodable by said instruction decoder attempting to make a memory access using a null value (Click column 1, line 66 to column 2, line 47; column 3, line 48 to column 4, line 7; and column 6, lines 45-67). Claims 21, 36, and 51 have similar limitations to claim 6 and are rejected for similar reasons. The only differences are that claim 21 is for a method and claims 36 and 51 are for a computer program product.

17. Referring to claims 7, 22, 37, and 52, taking claim 7 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, wherein said null value exception handler is operable to determine if said memory access instruction attempting to access a location corresponding to a null value corresponds to an error in operation of a virtual machine computer program operable to translate non-native program instructions that are not directly decodable by said instruction decoder into native program instructions that are directly decodable by said instruction decoder (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 22, 37, and 52 have similar limitations to claim 7 and are rejected for similar reasons. The only differences are that claim 22 is for a method and claims 37 and 52 are for a computer program product.

18. Referring to claims 8, 23, 38, and 53, taking claim 8 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 6, wherein said non-native program instructions are machine independent program instructions (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 23, 38, and 53 have similar

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limitations to claim 8 and are rejected for similar reasons. The only differences are that claim 23 is for a method and claims 38 and 53 are for a computer program product.

19. Referring to claims 9, 24, 39, and 54, taking claim 9 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 8, wherein said machine independent program instructions are one of:

- a. Java bytecodes (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7);
- b. MSIL bytecodes;
- c. CIL bytecodes; and
- d. .NET bytecodes.

20. Claims 24, 39, and 54 have similar limitations to claim 9 and are rejected for similar reasons. The only differences are that claim 24 is for a method and claim 39 and 54 are for a computer program product.

21. Referring to claims 10, 25, 40, and 55, taking claim 10 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 6, wherein said non-native instructions are native program instructions of a different apparatus for processing data (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 25, 40, and 55 have similar limitations to claim 10 and are rejected for similar reasons. The only differences are that claim 25 is for a method and claims 40 and 55 are for a computer program product.

22. Referring to claims 11, 26, 41, and 56, taking claim 11 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 10, wherein said processing logic and said instruction decoder are part of a RISC processor and said non-native instructions are native

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instructions of a CISC processor (Smith Abstract; column 1, lines 14-20; column 3, lines 9-20).

Claims 26, 41, and 56 have similar limitations to claim 11 and are rejected for similar reasons.

The only differences are that claim 26 is for a method and claims 41 and 56 are for a computer program product.

23. Referring to claim 14, 29, 44, and 59, taking claim 14 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, wherein said memory access instruction is a load instruction operable to load into a destination register specified by a destination register field within said load instruction a load value dependent upon a value read from a memory location specified by said base register value (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 29, 44, and 59 have similar limitations to claim 14 and are rejected for similar reasons. The only differences are that claim 29 is for a method and claims 44 and 59 are for a computer program product.

24. Referring to claims 15, 30, 45, and 60, taking claim 15 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, wherein said memory access instruction is a store instruction operable to store into a memory location specified by said base register value a store value dependent upon source value stored within a source register specified by a source register field within said store instruction (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 30, 45, and 60 have similar limitations to claim 15 and are rejected for similar reasons. The only differences are that claim 30 is for a method and claims 45 and 60 are for a computer program product.

25. Claims 2-5, 12-13, 17-20, 27-28, 32-35, 42-43, 47-50, and 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Click, Jr. et al., U.S. Patent Number 6,363,522 (herein

referred to as Click) in view of Smith et al., U.S. Patent Number 5,430,862 (herein referred to as Smith) as applied to claims 1, 16, 32, and 46 above, and further in view of Mirapuri et al., U.S. Patent Number 5,590,294 (herein referred to as Mirapuri).

26. Referring to claims 2, 17, 32, and 47, taking claim 2 as exemplary, Click in view of Smith has taught an apparatus as claimed in claim 1, but not taught wherein in response to said memory access instruction a return address is stored pointing a memory location storing a program instruction to be executed upon a return from said null value exception handler. Mirapuri has taught wherein in response to said memory access instruction a return address is stored pointing a memory location storing a program instruction to be executed upon a return from said null value exception handler (Mirapuri column 2, lines 41-51; column 7, lines 36-53; column 10, lines 15-41; column 12, line 53 to column 13, line 10; and Figure 8). A person of ordinary skill in the art at the time the invention was made, and as taught by Mirapuri, the device of Mirapuri improves pipeline throughput (Mirapuri column 3, lines 3-5), thereby improving processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the co-processing of Mirapuri in the device of Smith to improve processor efficiency and speed. Claims 17, 32, and 47 have similar limitations to claim 2 and are rejected for similar reasons. The only differences are that claim 17 is for a method and claims 32 and 47 are for a computer program product.

27. Referring to claims 3, 18, 33, and 48, taking claim 3 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 1, wherein said null value exception handler is located at a memory address pointed to by a value stored within a programmable configuration register (Mirapuri column 2, lines 41-51; column 7, lines

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36-53; column 10, lines 15-41; column 12, line 53 to column 13, line 10; and Figure 8). Claims 18, 33, and 48 have similar limitations to claim 3 and are rejected for similar reasons. The only differences are that claim 18 is for a method and claims 33 and 48 are for a computer program product.

28. Referring to claims 4, 19, 34, and 49, taking claim 4 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 3, wherein said programmable configuration register is a coprocessor configuration register (Mirapuri column 2, lines 41-51; column 7, lines 36-53; column 10, lines 15-41; column 12, line 53 to column 13, line 10; and Figure 8). Claims 19, 34, and 49 have similar limitations to claim 19 and are rejected for similar reasons. The only differences are that claim 19 is for a method and claims 34 and 49 are for a computer program product.

29. Referring to claims 5, 20, 35, and 50, taking claim 5 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 3, wherein said branch is made to an instruction stored at a memory address given by said value stored within said programmable configuration register subject to a fixed offset (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 20, 35, and 50 have similar limitations to claim 5 and are rejected for similar reasons. The only differences are that claim 20 is for a method and claims 35 and 50 are for a computer program product.

30. Referring to claims 12, 27, 42, and 57, taking claim 12 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 3, wherein said value stored within said programmable configuration register is a start address of said null value exception handler (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to

column 4, line 7). Claims 27, 42, and 57 have similar limitations to claim 12 and are rejected for similar reasons. The only differences are that claim 12 is for a method and claims 42 and 57 are for a computer program product.

31. Referring to claims 13, 28, 43, and 58, taking claim 13 as exemplary, Click in view of Smith and in further view of Mirapuri have taught an apparatus as claimed in claim 3, wherein said value stored within said programmable configuration register is an address of a jump instruction operable to jump execution to a start address of said null value exception handler (Click column 1, line 66 to column 2, line 47 and column 3, line 48 to column 4, line 7). Claims 28, 43, and 58 have similar limitations to claim 13 and are rejected for similar reasons. The only differences are that claim 13 is for a method and claims 43 and 58 are for a computer program product.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. Shpeisman et al., U.S. Patent Application Publication 2004/0268095, has taught a null reference check.
- b. Rodgers et al., U.S. Patent Number 5,889,982, has taught an exception handler.
- c. Ishizaki et al., U.S. Patent Number 6,484,314, has taught an exception handler that handles null exceptions.
- d. Dijkstra, U.S. Patent Number 6,789,098, has taught an exception handler with a compare and branch instruction.

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33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL

Aimee J. Li

4 May 2006


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